

WHAT IS CLAIMED IS:

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1. A method of generating a global history vector comprising the steps of:
 determining if a selected group of instructions contains a branch instruction;
 maintaining a current global history vector in a shift register when the selected group does not contain a branch instruction;
 shifting a first value into the shift register to generate a second vector if the selected group contains a branch instruction and the branch instruction is predicted as a branch taken; and
 shifting a second value into the shift register to generate a second vector when the selected group contains a branch instruction and the selected group does not include a branch instruction predicted as a branch taken.
 2. The method of Claim 1 and further comprising the step of storing the generated value in an entry in a branch instruction queue associated with the selected group of instructions.
 3. The method of Claim 2 and further comprising the step of correcting the generated vector upon a misprediction comprising the substeps of:
 retrieving a selected number of bits of the vector stored from the branch instruction queue into the shift register; and
 shifting an updated history bit into the shift register.
 4. The method of Claim 1 wherein the first value comprises a logic 1 and the second value is a logic 0.



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1 6. A method of performing branch predictions comprising the steps of:
2 indexing a branch history table using a first global history vector associated with
3 a first fetch group of instructions during a first fetch cycle to retrieve a first prediction
4 value;
5 generating a second global history vector associated with a second fetch group
6 of instructions comprising the substeps of
7 retaining the first vector when the first fetch group does not contain at
8 least one branch instruction;
9 appending a bit of a first value to the first vector when the first fetch
10 group has at least one branch instruction predicted to be a branch taken; and
11 appending a bit of a second value to the first vector when the first group
12 contains at least one branch instruction and contains no branch instructions
13 predicted to be a branch taken; and
14 indexing the branch history table using the second global history vector during
15 a second fetch cycle to retrieve a second branch prediction value.

1 7. The method of Claim 6 and further comprising the step of storing the first and
2 second vectors in an entry of a branch history queue associated with the with the first
3 fetch group.

1 8. The method of Claim 7 and further comprising the steps of:
2 detecting a branch misprediction based on the first prediction value;
3 retrieving the first and second vectors from the branch history queue;
4 indexing the branch history table using the first vector to correct the first
5 prediction value; and

6 appending a corrected bit to the second vector to generate a corrected branch
7 history vector.

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1 9. The method of Claim 7 wherein said first fetch cycle precedes the second fetch
2 cycle by three fetch cycles.

1 10. The method of Claim 7 wherein said steps of indexing comprises the step of
2 gating the vector with selected bits of a current instruction address.

1 11. The method of Claim 10 wherein said steps of gating comprise the steps of
2 performing XOR operations.

1 12. The method of Claim 8 wherein said substeps of appending comprise the
2 substeps of shifting a bit into a shift register storing the first vector.

1 13. Branch processing circuitry comprising:
2 a shift register for storing a global history vector;
3 control circuitry for selectively updating a first global history vector stored in said
4 shift register operable to:

5 determine if a selected group of instructions contains a branch
6 instruction;

7 maintain said first global history vector in said shift register when the
8 selected group does not contain a branch instruction;

9 shift a first value into the shift register to generate a second vector if the
10 selected group contains a branch instruction and the branch instruction is
11 predicted as a branch taken; and

12 shifting a second value into the shift register to generate a second vector
13 when the selected group contains a branch instruction and does not contain a
14 branch instruction predicted as a branch taken.

1 14. The branch processing circuitry of Claim 13 and further comprising a branch
2 history table and circuitry for generating an index to an entry in said branch history table
3 using selected bits from a current address and selected bits of said first vector to retrieve
4 a prediction value stored therein.

1 15. The branch processing circuitry of Claim 14 and further comprising circuitry for
2 updating said second vector when said prediction value results in a misprediction
3 comprising:

4 a queue for storing said first and said second vectors;
5 circuitry for accessing said vectors from said queue;

16. The branch processing circuitry of Claim 13 wherein said branch processing circuitry forms a portion of a single-chip microprocessor.

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- 1 17. A processing system comprising:
2 a microprocessor comprising:
3 a branch history table for storing branch prediction values;
4 a global history shift register for storing a global branch history vector;
5 logic for generating an index to said branch history table and accessing
6 prediction values stored therein using selected bits of a said branch history vector
7 stored in said shift register; and
8 control circuitry for updating a said global branch history vector stored
9 in said shift register and operable to:
10 retain a current vector stored in said shift register when a selected
11 fetch group does not contain at least one branch instruction;
12 shift a bit of a first value into said shift register to generate an
13 updated vector when the selected fetch group has at least one branch
14 instruction predicted to be a branch taken; and
15 shift a bit of a second value into said shift register when said
16 selected fetch group contains at least one branch instruction and contains
17 no branch instructions predicted to be a branch taken.

- 1 18. The processing system of Claim 17 wherein said microprocessor further
2 comprises :
3 a branch instruction queue having a plurality of entries each associated with a
4 said fetch group for storing at least first and second corresponding global history vectors;
5 circuitry for detecting a misprediction associated with a said prediction value
6 retrieved from said branch history table and corresponding to said first global history
7 vector in said branch instruction queue;

8 circuitry for retrieving said first vector from said branch instruction queue and
9 accessing a corresponding entry in said branch history table to correct said prediction
10 value stored therein; and

11 circuitry for retrieving and modifying said second vector to generate a corrected
12 vector in said shift register.

1 19. The processing system of Claim 17 wherein said processing system further
2 includes a system memory coupled to said microprocessor by a bus.

1 20. The processing system of Claim 17 wherein a said fetch group comprises eight
2 instructions.